PCB Layout and Design Guide for CH7025/CH7026 TV/VGA Encoder

1.0 Introduction

The CH7025/CH7026 is a device targeting handheld and similar systems which accept a digital input signal, and encodes and transmits data through three 10-bit DACs. The device is able to encode the video signals and generate synchronization signals for NTSC and PAL standards. Analog RGB output and composite SYNC signal are also supported. The device accepts different data formats including RGB and YCrCb (e.g. RGB565, RGB666, RGB888, ITU656 like YCrCb, etc.). 16Mbit SDRAM can is embedded in package, so Frame rate conversion and Image Rotation are possible.

This application note focuses only on the basic PCB layout and design guidelines for CH7025/CH7026 TV/VGA encoder. Guidelines in component placement, power supply decoupling, grounding, input/output signal interface are discussed in this document.

The discussion and figures that follow reflect and describe connections based on the 80-pin LQFP and BGA package of the CH7025/CH7026. Please refer to the CH7025/CH7026 datasheet for the details of the pin assignments.

2.0 Component Placement and Design Considerations

Components associated with the CH7025/CH7026 should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1μF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C1, C2, C3, C4, C5, C6, C7) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7025/CH7026 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7025/CH7026 should be connected to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7025/CH7026 ground pins should be connected to its respective decoupling capacitor ground lead directly, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. Refer to **Table 1** and **Table 2** for the Ground pins assignment.

2.1.2 Power Supply Pins

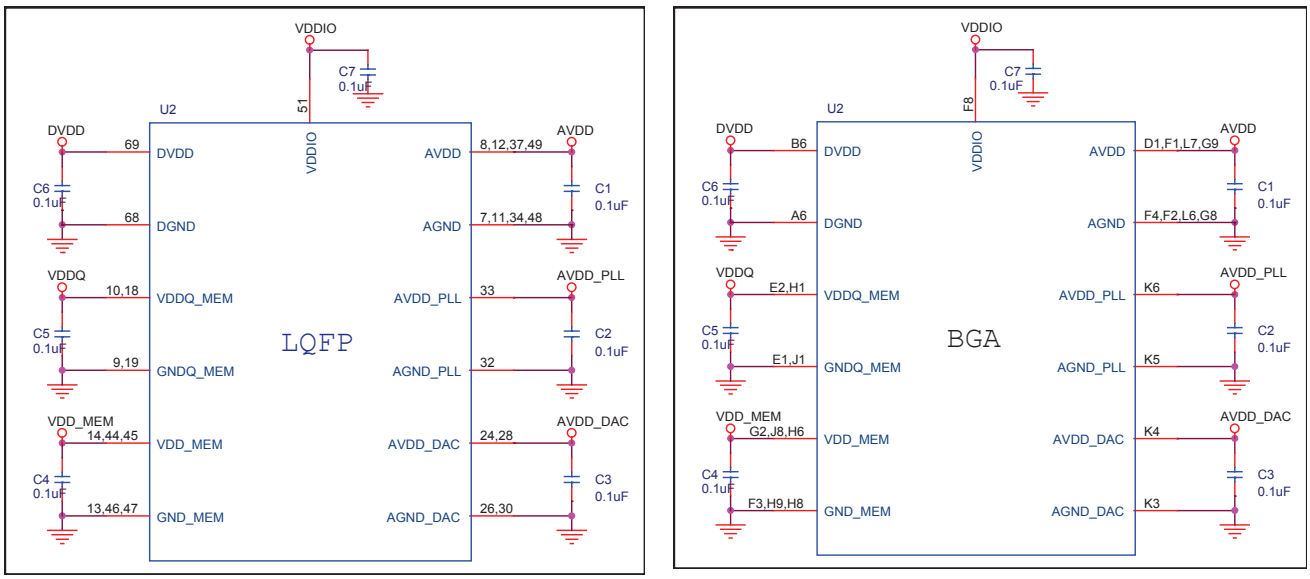
There are seven power supply pins, AVDD, AVDD_DAC, AVDD_PLL, VDDIO, DVDD, VDDQ, VDD_MEM. Refer to **Table 1** and **Table 2**for the Power supply pins assignment. Refer to **Figure 1** for Power Supply Decoupling.

Table 1: Power Supply Pins Assignment of the CH7025/CH7026(LQFP)

Pin Assignment	# of Pins	Type	Symbol	Description
51	1	Power	VDDIO	IO supply voltage (1.2-3.3V)
69	1	Power	DVDD	Digital supply voltage (1.8V)
8,12,37,49	4	Power	AVDD	Analog supply voltage (2.5 – 3.3V)
33	1	Power	AVDD_PLL	PLL supply voltage (1.8V)
24,28	2	Power	AVDD_DAC	DAC power supply (2.5 – 3.3V)
10,18	2	Power	VDDQ_MEM	SDRAM output buffer supply voltage (2.5V)
14,44,45	3	Power	VDD_MEM	SDRAM device supply voltage (2.5V)
68	1	Ground	DGND	Digital supply ground
7,11,34,48	4	Ground	AGND	Analog supply ground
32	1	Ground	AGND_PLL	PLL supply ground
26,30	2	Ground	AGND_DAC	DAC supply ground
9,19	2	Ground	GNDQ	SDRAM output buffer supply ground
13,46,47	3	Ground	GND_MEM	SDRAM device supply ground

Table 2: Power Supply Pins Assignment of the CH7025/CH7026 (BGA)

Pin Assignment	# of Pins	Type	Symbol	Description
F8	1	Power	VDDIO	IO supply voltage (1.2-3.3V)
B6	1	Power	DVDD	Digital supply voltage (1.8V)
D1, F1, L7, G9	4	Power	AVDD	Analog supply voltage (2.5 – 3.3V)
K6	1	Power	AVDD_PLL	PLL supply voltage (1.8V)
K4	1	Power	AVDD_DAC	DAC power supply (2.5 – 3.3V)
E2, H1	2	Power	VDDQ	SDRAM output buffer supply voltage (2.5V)
G2, J8, H6	3	Power	VDD_MEM	SDRAM device supply voltage (2.5V)
A6	1	Ground	DGND	Digital supply ground
F4, F2, L6, G8	4	Ground	AGND	Analog supply ground
K5	1	Ground	AGND_PLL	PLL supply ground
K3	1	Ground	AGND_DAC	DAC supply ground
E1, J1	2	Ground	GNDQ	SDRAM output buffer supply ground
F3, H9, H8	3	Ground	GND_MEM	SDRAM device supply ground



(a) LQFP Package (b) BGA Package

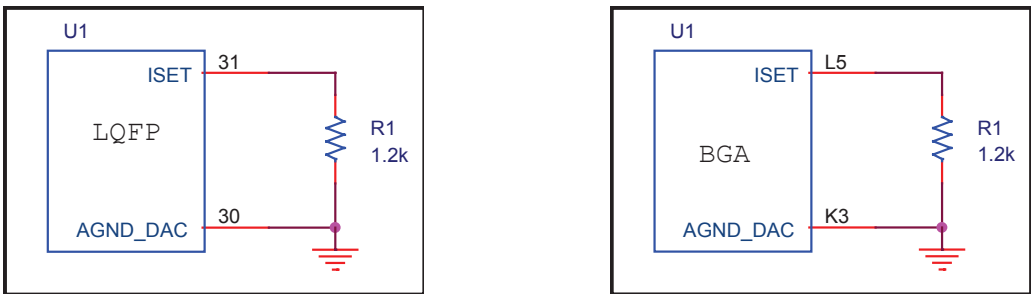
Figure 1: Power Supply Decoupling and Distribution

Note: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05 Ω at DC; 23 Ω at 25MHz & 47 Ω at 100MHz. Please refer to Fair Rite part #2743019447 for details or an equivalent part can be used for the diagram.

2.2 Internal Reference Pins

• ISET pin

This pin sets the DAC current. A 1.2 kΩ, 1% tolerance resistor should be connected between ISET and AGND_DAC as shown in **Figure 2**. A smaller resistance will create more DAC current, resulting brighter TV out images. This resistor should be placed with short and wide traces as near as possible to CH7025/CH7026.



(a) LQFP Package **(b) BGA Package**

Figure 2: ISET pin connection

2.3 General Control Pins

• RESETB

This pin is the chip reset pin for CH7025/CH7026. RESETB pin, which is internally pulled-up, places the device in the power on reset condition when this pin is low. A power reset switch can be placed on the RESETB pin on the PCB as a hardware reset for CH7025/CH7026 as shown in **Figure 3**. When the pin is high, the reset function can also be controlled through the serial port.

• XI and XO

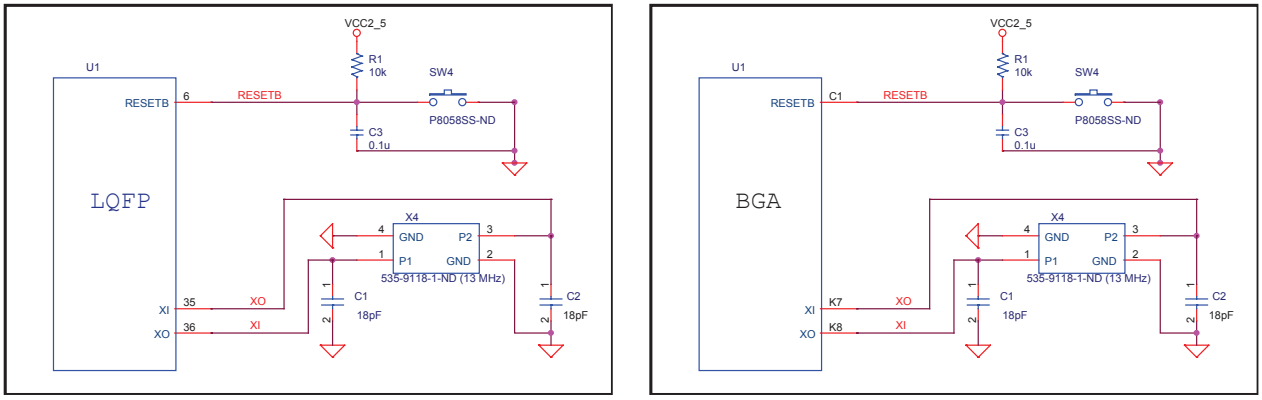
CH7025/CH7026 has capability to accept external clocks with frequencies from 2.3 MHz to 64 MHz. However, we recommend predefined crystal frequencies as stated in the CH7025/CH7026 datasheet for the crystal or oscillator.

Predefined crystal frequencies used for CH7025/CH7026 are shown in **Table 3.** The crystal selection register is located at Register 41h.

Table 3: Predefined Crystal Frequencies

XTAL[3:0]	Frequency
0	3.6864MHz
1	3.579545MHz
2	4MHz
3	12MHz
4	13MHz
5	13.5MHz
6	14.318MHz
7	14.7456MHz
8	16MHz
9	18.432MHz
10	20MHz
11	26MHz
12	27MHz
13	32MHz
14	40MHz
15	49MHz

The crystal load capacitance, C_L, is usually specified in the crystal spec from the vendor. As an example to show the load capacitors **Figure 3** gives a reference design for crystal circuit design.



(a) LQFP Package (b) BGA Package

Figure 3: General Control Pins

• Reference Crystal Oscillator

CH7025/CH7026 includes an oscillator circuit that allows a predefined-frequency crystal to be connected directly. Alternatively, an externally generated clock source may be supplied to CH7025/CH7026. If an external clock source is used, it should have CMOS level specifications. The clock should be connected to the XI pin, and the XO pin should be left open. The external source must exhibit ±20ppm or better frequency accuracy, and have low jitter characteristics.

If a crystal is used, the designer should ensure that the following conditions are met:

The crystal is specified to be predefined-frequency, ±20 ppm fundamental type and in parallel resonance (NOT series resonance). The crystal should also have a load capacitance equal to its specified value (C_L).

External load capacitors have their ground connection very close to CH7025/CH7026 (C_{ext}).

To be able to tune, a variable capacitor may be connected from XI to ground.

Note that the XI and XO pins each has approximately 10 pF (C_{int}) of shunt capacitance internal to the device. To calculate the proper external load capacitance to be added to the XI and XO pins, the following calculation should be used:

$\mathbf{C}_{ext} = (2 \times C_L) - C_{int} - 2C_S$

where
C_{ext} = external load capacitance required on XI and XO pins.

C_L = crystal load capacitance specified by crystal manufacturer.

C_{int} = capacitance internal to CH7025/CH7026 (approximately 10-15 pF on each of XI and XO pins).

C_S = stray capacitance of the circuit (i.e. routing capacitance on the PCB, associated capacitance of crystal holder from pin to pin etc.).

In general,
$C_{int}XI = C_{int}XO = C_{int}$
$C_{ext}XI = C_{ext}XO = C_{ext}$

such that
$C_L = (C_{int} + C_{ext}) / 2 + C_S$ and $C_{ext} = 2 (C_L - C_S) - C_{int} = 2C_L - (2C_S + C_{int})$

Therefore C_L must be specified greater than $C_{int} /2 + C_S$ in order to select C_{ext} properly.

After C_L (crystal load capacitance) is properly selected, care should be taken to make sure the crystal is not operating in an excessive drive level specified by the crystal manufacturer. Otherwise, the crystal will age quickly and that in turn will affect the operating frequency of the crystal.

For detail considerations of crystal oscillator design, please refer to **AN-06**.

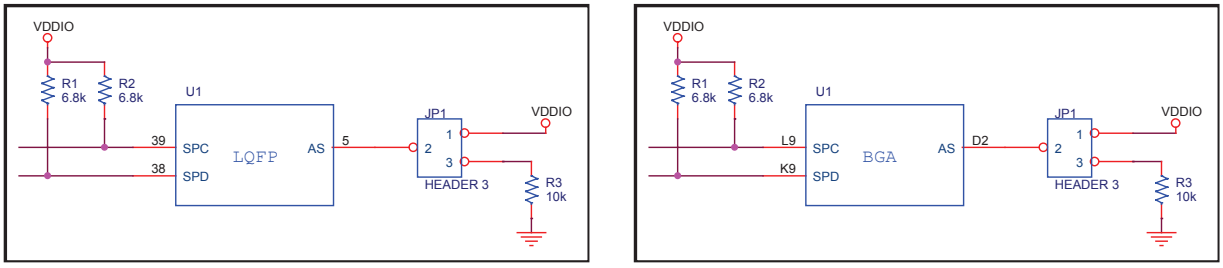
2.4 Serial Port Control for CH7025/CH7026

• SPC and SPD

SPD and SPC function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC pins are pulled up to VDDIO (+1.2V ~ +3.3V) with 6.8kΩ resistors as shown in **Figure 4**.

• AS

This pin determines the serial port address of CH7025/CH7026. Address = 75h when AS is high. Address = 76h when AS is low. See **Figure 4** for detail.



(a) LQFP Package **(b) BGA Package**

Figure 4: Serial Port Control

2.5 Input Pins

• Data Inputs

CH7025/CH7026 can accept up to 24 data inputs, as shown in **Figure 5**, from a digital video port of a graphics controller. The swing is defined by VDDIO (1.2 ~ 3.3V).
Unused Data input pins should be pulled low with 10kΩ resistors or shorted to Ground directly.

• H/V Sync Pins

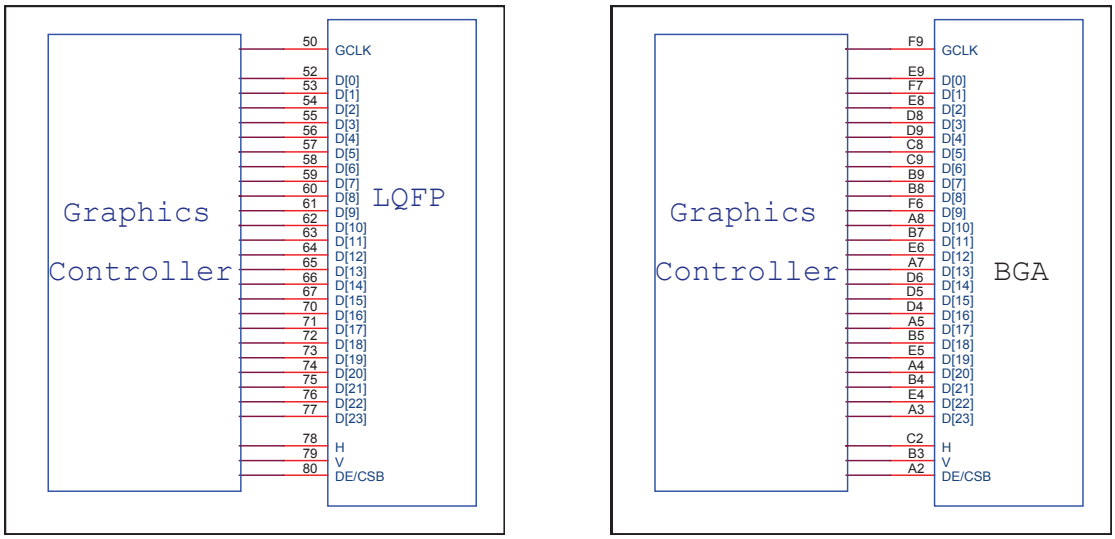
The horizontal/vertical sync pins can be used as inputs as shown in **Figure 5**.

• DE/CSB

The DE/CSB pin is used as a data input indicator (See **Figure 5**). When the pin is high, the input data is active. When the pin is low, the input data is blanking.
If DE/CSB is not used, it can be left open or pulled down to the Ground.

• GCLK

The GCLK input is the clock signal input to the device for using with the H, V, DE and D[23:0] data.



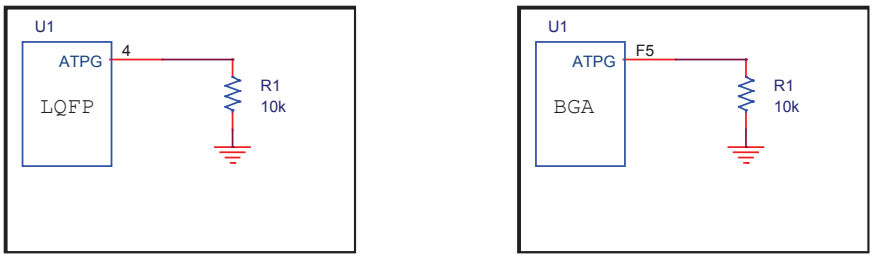
(a) LQFP Package **(b) BGA Package**

Figure 5: CH7025/CH7026 Input Pins

2.6 Miscellaneous Pins

• ATPG

The ATPG pin should be left open or pulled low with a 10kΩ resister in the application as shown in **Figure 6**.



(a) LQFP Package **(b) BGA Package**

Figure 6: ATPG Pin

2.7 Video Outputs

• TV DAC0~2 output

Three on-chip 10-bit high speed DACs provide flexible output capabilities, such as single, double or triple CVBS output, simultaneous CVBS and S-video output. If the DACs require a double termination, a 75 Ω resistor should be placed between each DAC pin and the ground as shown in **Figure 7**.

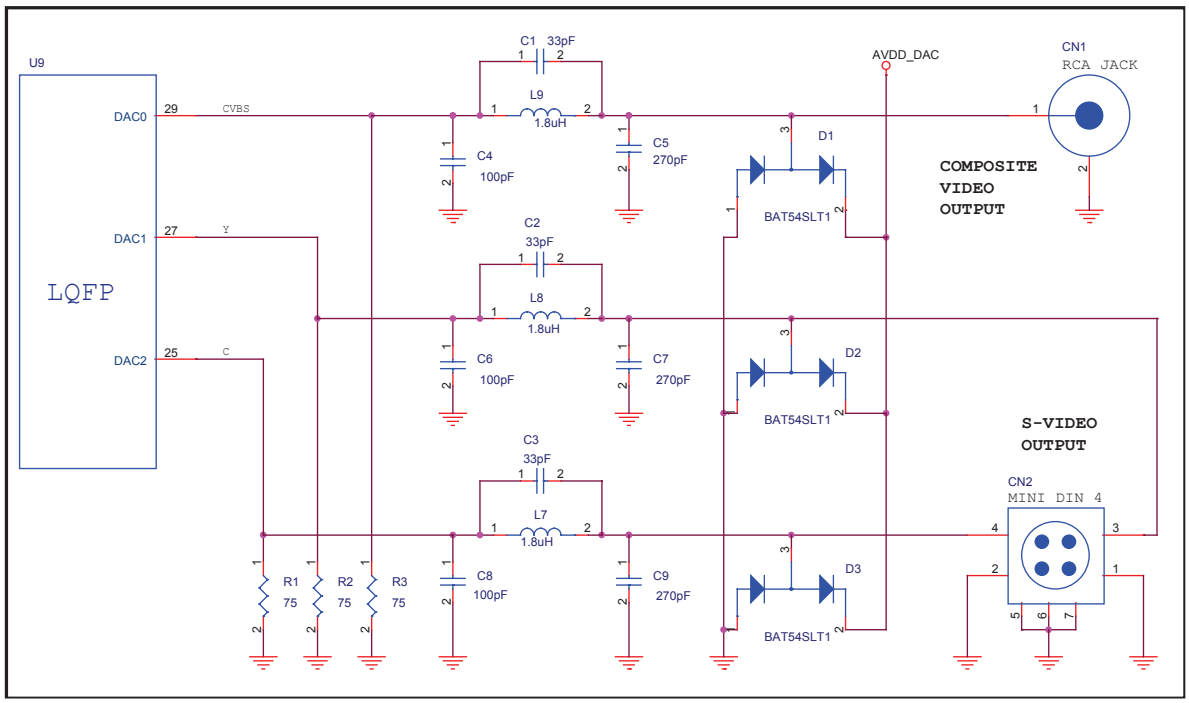


Figure 7(a): CH7025/CH7026 Video Output - LQFP

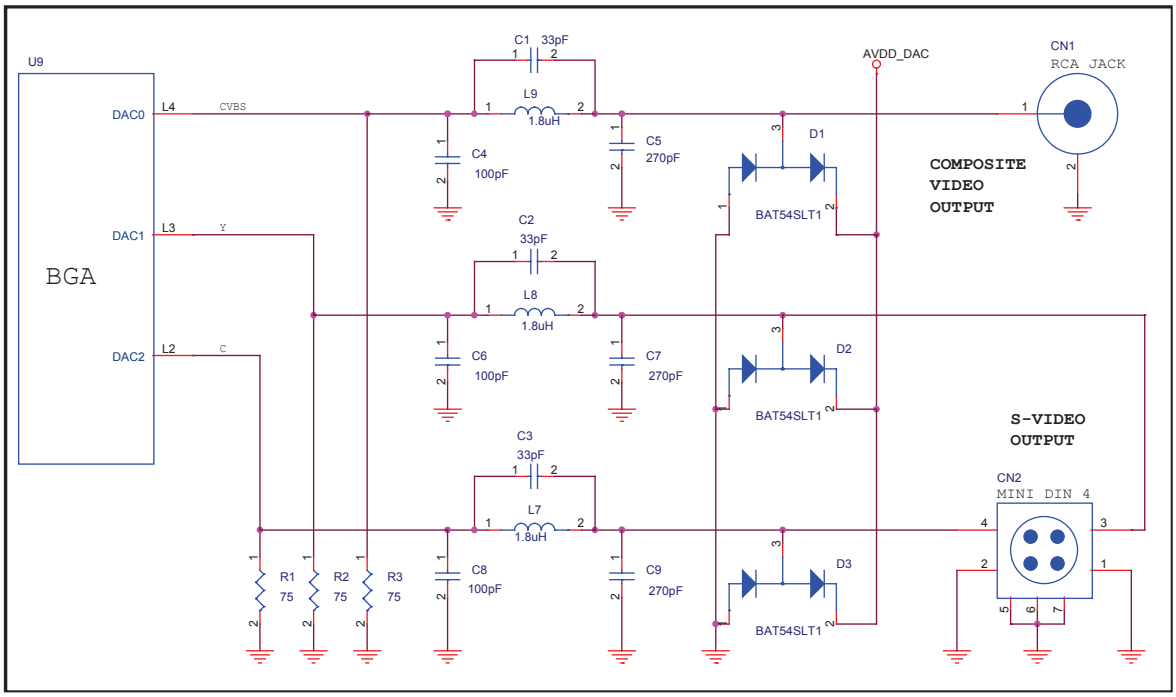


Figure 7(b): CH7025/CH7026 Video Output – BGA

- **YPbPr and RGB+Csync output**

CH7026B support both SDTV and HDTV YPbPr output format. The resolution is from 480i to 720p and 1080i. In RGB+Csync output format, the Csync high level is the same with AVDD power supply. Csync pin is a COMS push-pull output pin, customer can use other circuit to change is high level to 0.7V or other voltage level according to different Receivers.

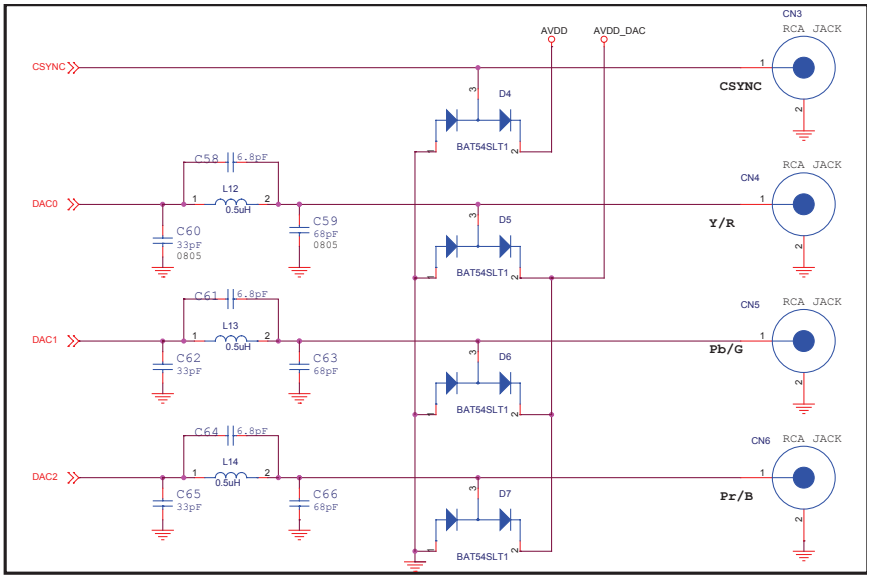


Figure 8: CH7025/CH7026 YPbPr and RGB+Csync output

- **VGA output**

VGA standard output signal level of Hsync and Vsync is more than 2.4V. CH7026B Hsync and Vsync output signal level is same with AVDD power supply. Customer can use 74ACT08 (AND GATE) to pull high this signal level to 5V. It is recommended but not necessary.

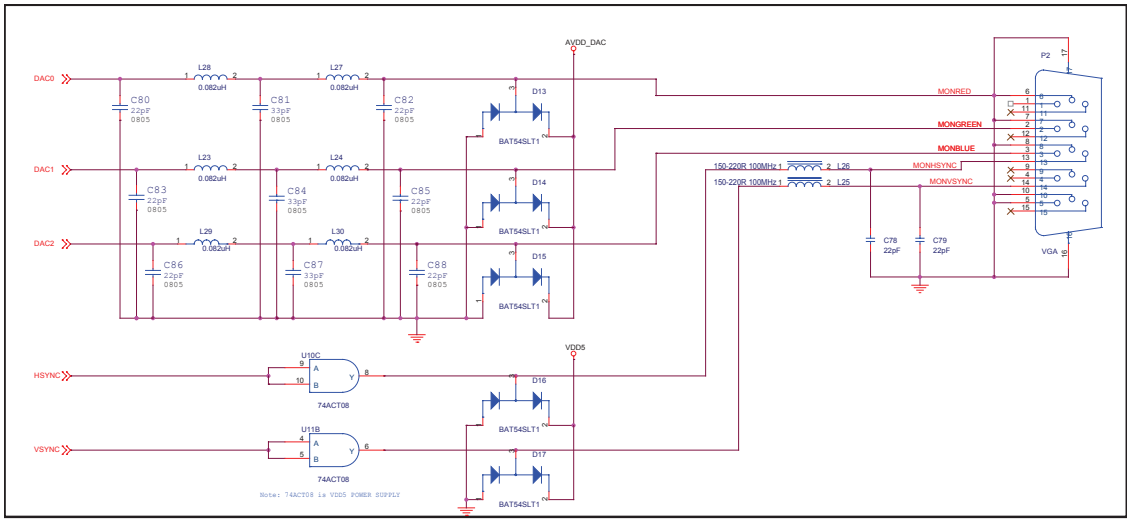


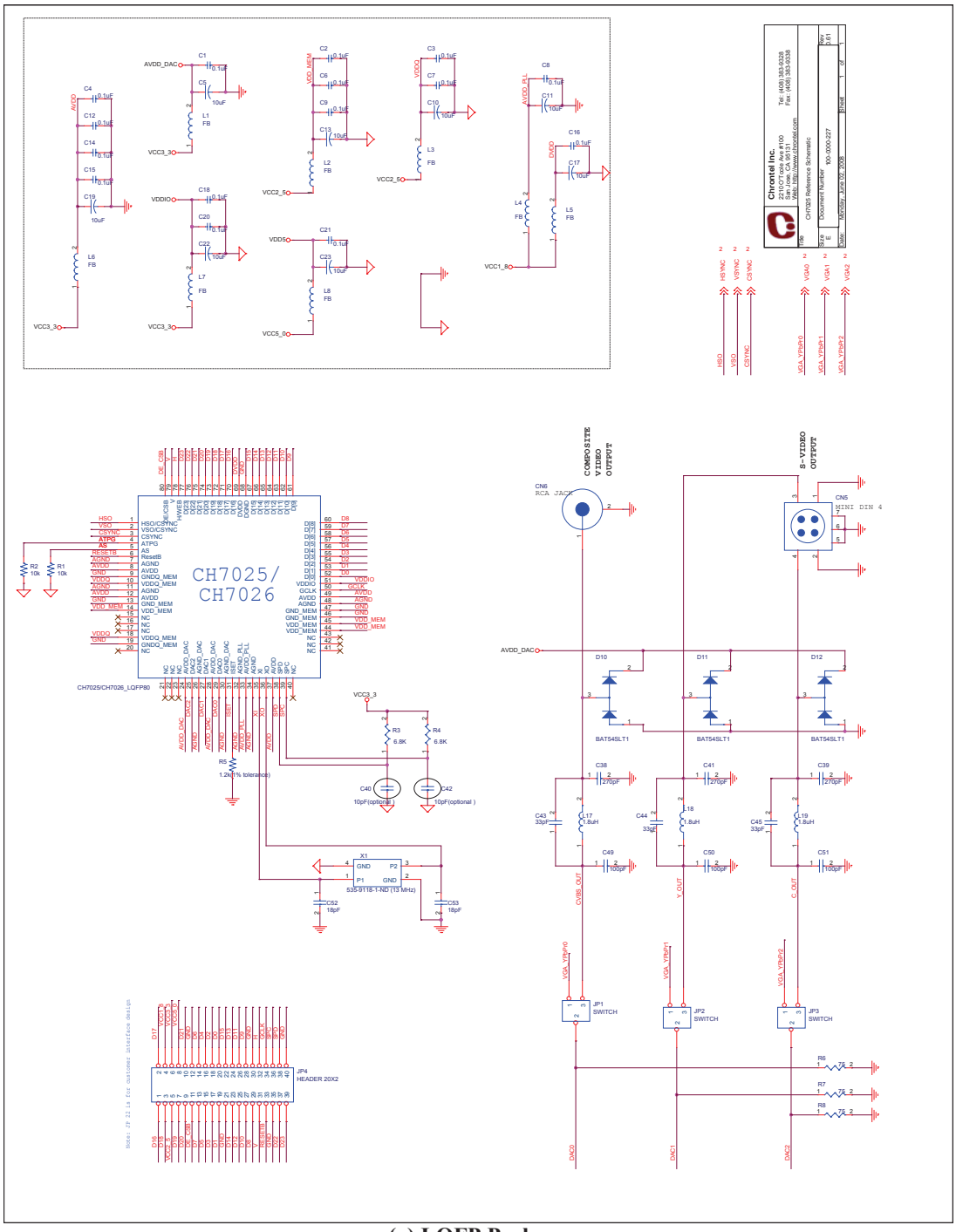
Figure 9: CH7025/CH7026 VGA Hsync and Vsync output

Note: In order to minimize the hazard of ESD, a set of protection diodes (BAT54SLT1) are highly recommended for each DAC and Sync Output.

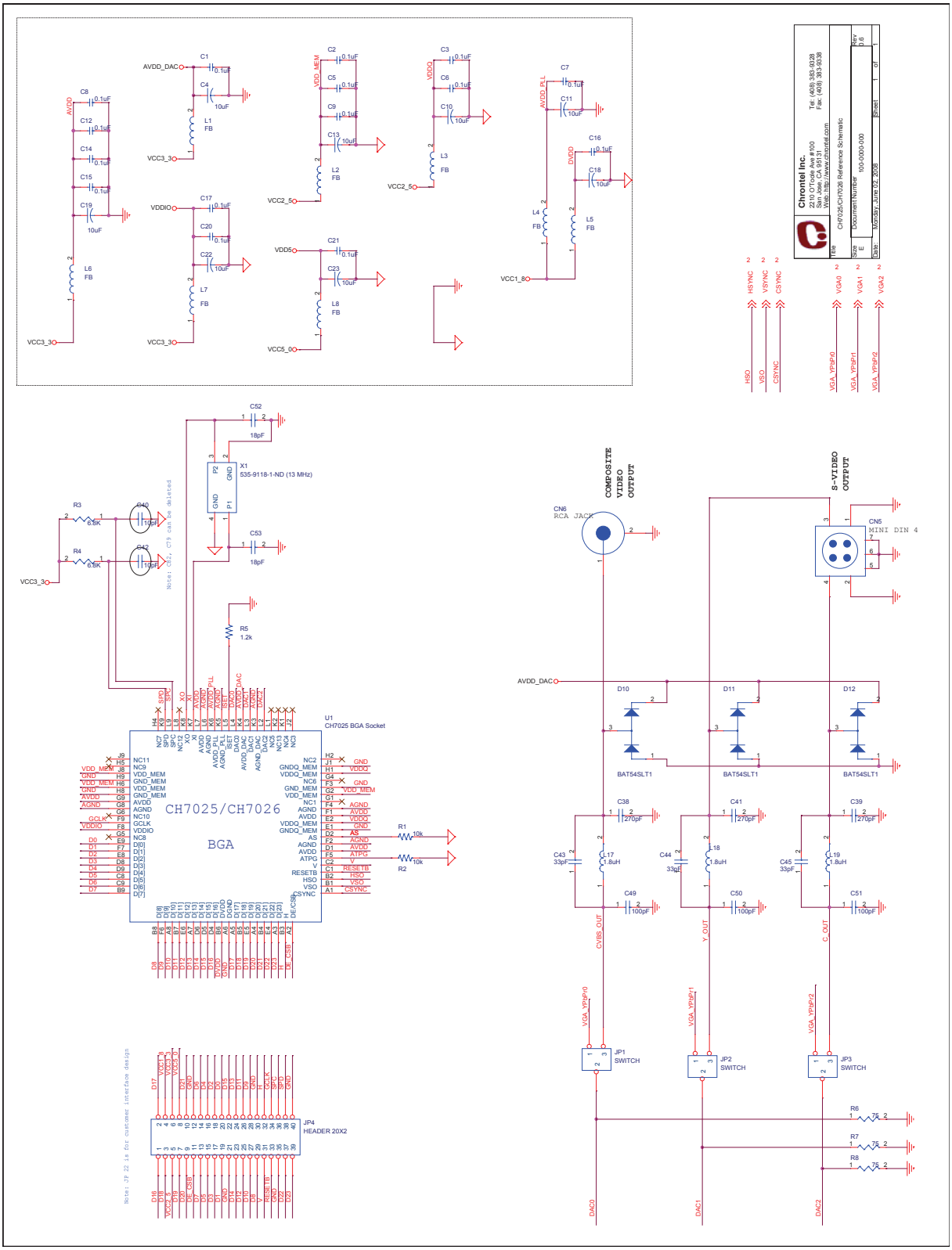
3.0 Reference Design Example

The figures below are the reference schematic of CH7025/CH7026, which is provided here for design reference only. We encourage those who will engage in an application design with CH7025/CH7026 to contact Chrontel Applications group. **Table 4** provides the BOM list for the reference schematic.

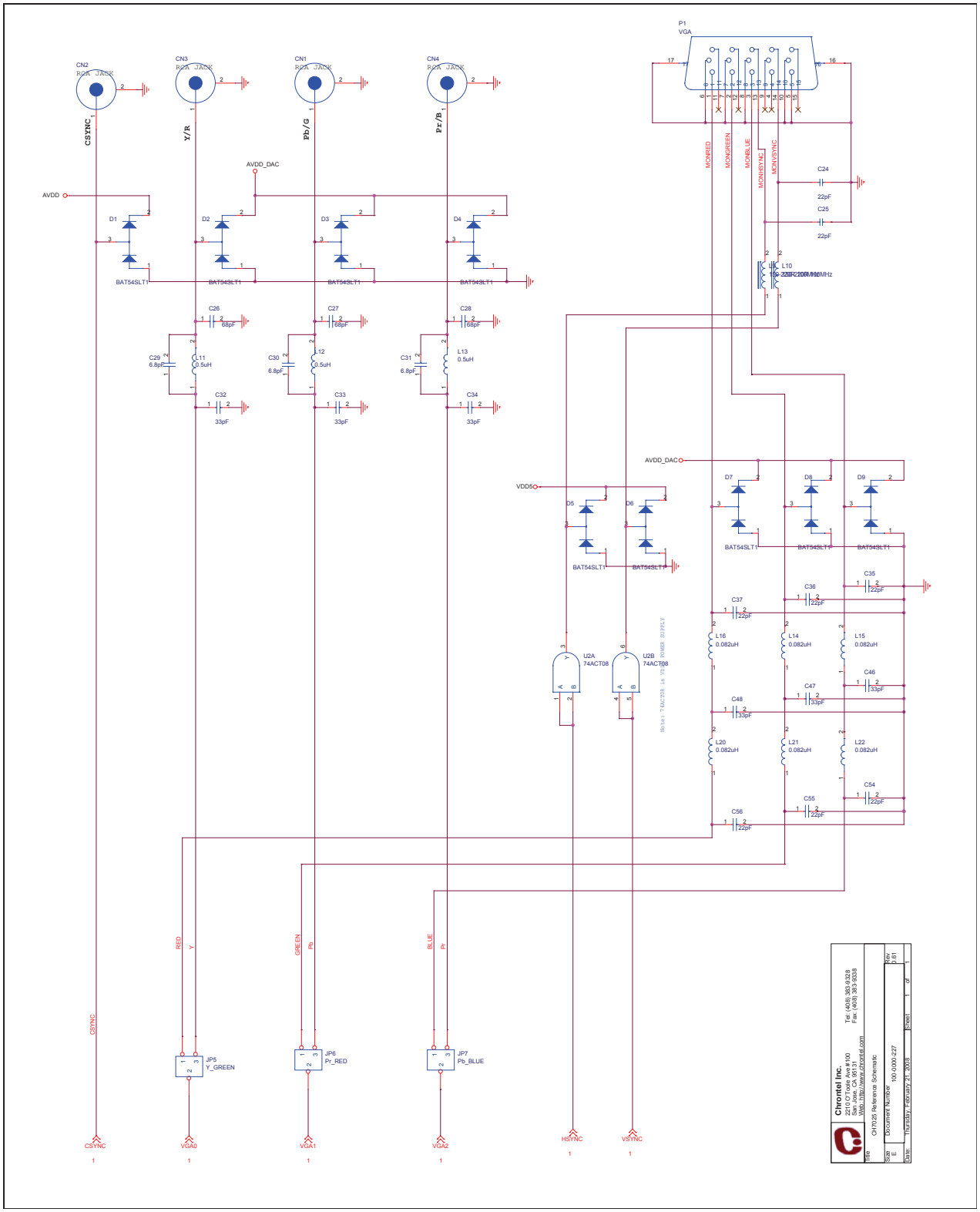
3.1 Reference Schematic



(a) LQFP Package



(b) BGA Package



(c) Output filter

3.2 Reference Board Preliminary BOM

Table 4: CH7025/CH7026 Reference Design BOM List

Item	Quantity	Reference	Part
1	5	CN1,CN2,CN3,CN4,CN6	RCA Jack
2	1	CN5	4-pin Mini DIN
3	15	C1,C2,C3,C4,C6,C7,C8,C9,	0.1uF
		C12,C14,C15,C16,C18,C20,	
		C21	
4	8	C5,C10,C11,C13,C17,C19,	10uF
		C22,C23	
5	8	C24,C25,C35,C36,C37,C54,	22pF
		C55,C56	
6	3	C26,C27,C28	68pF
7	3	C29,C30,C31	6.8pF
8	9	C32,C33,C34,C43,C44,C45,	33pF
		C46,C47,C48	
9	3	C38,C39,C41	270pF
10	2	C40,C42	10pF(optional)
11	3	C49,C50,C51	100pF
12	2	C52,C53	18pF
13	12	D1,D2,D3,D4,D5,D6,D7,D8,	BAT54SLT1
		D9,D10,D11,D12	
14	3	JP1,JP2,JP3	SWITCH
15	1	JP4	HEADER 20X2
16	1	JP5	Y_GREEN
17	1	JP6	Pr_RED
18	1	JP7	Pb_BLUE
19	8	L1,L2,L3,L4,L5,L6,L7,L8	FB
20	2	L9,L10	150-220R 100MHz
21	3	L11,L12,L13	0.5uH
22	6	L14,L15,L16,L20,L21,L22	0.082uH
23	3	L17,L18,L19	1.8uH
24	1	P1	VGA
25	2	R1,R2	10k
26	2	R3,R4	6.8K
27	1	R5	1.2k(1% tolerance)
28	3	R6,R7,R8	75ohm
29	1	U1	CH7025/CH7026_LQFP80
30	1	U2	74ACT08
31	1	X1	535-9118-1-ND (13 MHz)

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